Small-Signal Stability Analysis with Approximated PV Model for Solar Array Simulator

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***Abstract*—Solar array simulators (SAS) equipment is used to mimic the characteristics curve for PV generators. However, an in-depth stability analysis of the SAS with respect to its reference signal is yet to be investigated. This is due to implicit and non-linear mapping equations used to describe the I-V curve, which complicates the loop analysis. Our study proposes a super-elliptical method to approximate the I-V characteristic curve and provide an explicit PV equation that is straightforward to manipulate. Furthermore, this approximate model is then used for the dynamic performance assessment for the typical control architecture. Based on the comparative study using the approximate mode either in the theoretical analysis and the experimental verification, the resistance-sensing control scheme tends to reduce the effect of loop interactions in the SAS, thereby showing more consistent dynamic performance than the other control structure.**

***Index Terms*—PV Modeling, Solar Array Simulators, Small-Signal Model**

I. Introduction

Solar Array Simulators (SAS) are used to imitate the behavior of photovoltaic (PV) panels under varying irradiation and temperatures. SAS consists of a DC/DC converter, a reference generator, and a controller, as indicated in Fig. 1. A PV equation or look-up table is always embedded into the reference generator to ensure that the SAS output and I-V characteristics curve correspond [1].

The hardware control structures of SAS can be categorized based on its control and sensing method. The control method can either be the Voltage Reference Control (VRC) or the Current Reference Control (CRC), as shown in Fig. 2. Whereas the CRC utilizes the current reference signal generated from a sensed voltage, the reference signal in VRC is produced from a sensed current. Depending on its operating points, the DC/DC converter should operate as either a current or voltage source, where the dynamic response can be intensely dependent on the control structure in the current source segment (CSS) and voltage source segment (VSS) shown in Fig. 3. Most commercially available SAS seek stable and accurate points for their operation in the I- V curve. A detailed classification of the various hardware typologies currently in use is shown in Table I.

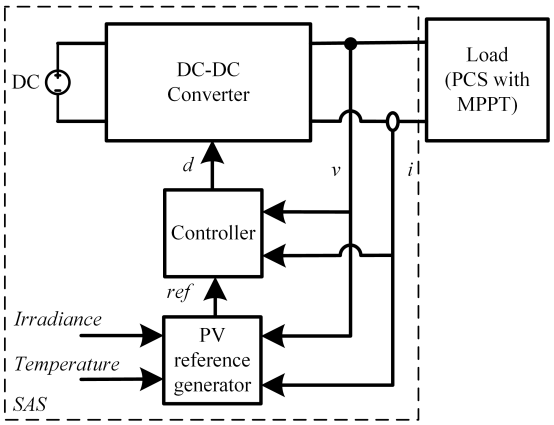


Fig. 1: A typical SAS system

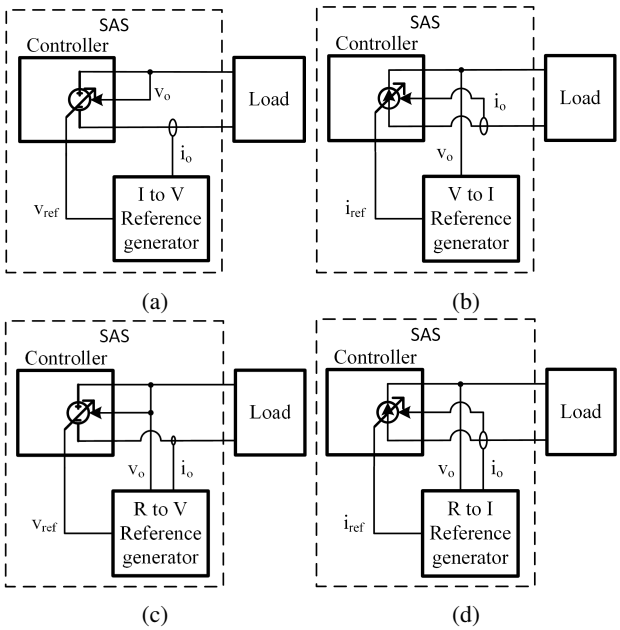


Fig. 2: Block diagrams of SAS configuration (a) CS-VRC (b) VS-CRC (c) RS-VRC (d) RS-CRC

The SAS sensing method can either be a voltage sensing (VS) [1]–[10], current sensing (CS) [15]–[18] or a resistance sensing (RS) [11]–[14]. Regardless of the sensing method used, the reference generator induces the reference signal according to the look-up table or approximate I-V characteristic equation embedded into the circuit. Some recent studies proposed a more advanced sensing method that combines VS, CS, and RS sensing methods to form a hybrid sensing method [19]–[21].

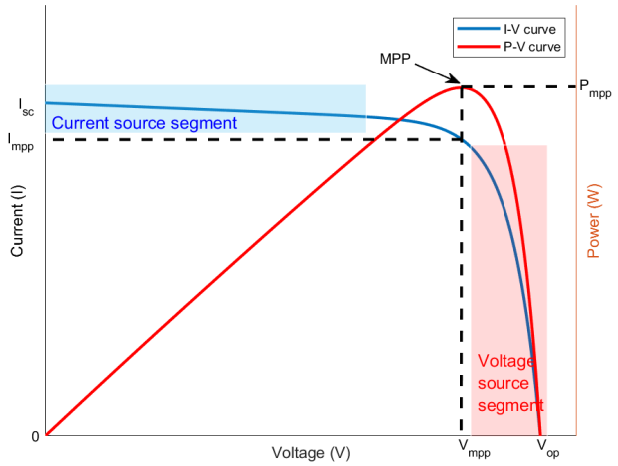


Fig. 3: Typical characteristic of the PV curve

TABLE I: Previous studies on SAS architecture

Ref.	Structure	Reference Generator	Controller
[1]	VS-CRC	PV equation	FS-MPC
[2]	VS-CRC	PV equation	PI
[3]	VS-CRC	Reference PV cell	PI
[4]	VS-CRC	Lookup table	PID
[5]	VS-CRC	Lookup table	PID
[6]	VS-CRC	Lookup table	Current mode PI
[7]	VS-CRC	Lookup table	PI
[8]	VS-CRC	PV equation	Peak voltage controlled PI
[9]	VS-CRC	PV equation	PI
[10]	VS-CRC	PV equation	FOPI
[11]	RS-CRC	PV equation	Current mode PI
[12]	RS-VRC	Lookup table	Boundary control law
[13]	RS-VRC	PV equation	Backstepping
[14]	RS-VRC	PV equation	PI or FLC
[15]	CS-VRC	Lookup table	FLC
[16]	CS-VRC	Lookup table	Current mode PI
[17]	CS-VRC	PV equation	Type III
[18]	CS-VRC	PV equation	PI
[19]	Hybrid (VS, RS-CRC)	Lookup table	PID
[20]	Hybrid (VS-CRC, CS-VRC)	Lookup table	PID
[21]	Hybrid (VS-CRC, CS-VRC,RS-VRC)	PV equation	PI

Although the reference generator of most commercial SAS is primarily based on predefined values stored in a look-up table, the resilience of the I-V characteristics curve is significantly reduced. The equation-based SAS offers more flexibility than a look-up table. However, it requires iterations to solve the implicit I-V relation. The Lambert-W function [10], [22], [23] which also requires long and complex iterations . Especially in [10], Lambert-W function PV reference generator and fractional-order PI (FOPI) controller are used and got comparatively better I-V curve but still has a deviation in CCS.

Due to this complexity, various studies have focused significantly on understanding the steady-state accuracy and inner loop interactions of the SAS under a constant load condition [21], [24]. Hence, for either a VRC or CRC hardware structure, only the voltage and current controllers were studied, respectively. However, the reference signal being a time-varying quantity reflects changes in its output into the SAS, disturbing overall system dynamics. Even though various studies have raised this opinion, not enough comprehensive and detailed explanation has been given. Specifically, the stability analysis and performance comparison of the different SAS hardware structures have a lack of research focus [19]–[21].

In this study, the various hardware structures of SAS are evaluated and compared with respect to multi-loop stability. Section II proposes the super-elliptical method as an approximation method for solving the implicitness of the PV characteristic equation; Section III discusses the small-signal model of the various hardware structures describing it as a multi-loop system. Section IV examines the multi-loop analysis based on these models. In addition, theoretical analysis confirming simulation results is indicated in Section VI presents the conclusions based on these results.

II. Modeling of PV Reference Generator

A. Elliptical Approximation for I-V Characteristics of PV Panels

The reference signal of an equation-based SAS is generated from a sensed variable based on the PV characteristics equation. The PV panel is modeled by an equivalent circuit consisting of a current source, two resistors, and a PN junction diode. The mathematical equation describing the characteristic curve of a PV panel becomes complex and implicit due to the exponential function. As a result, the iterative solutions for the module output voltage and current often require complicated and long expressions. The basic implicit equation for a PV generator is given as:

$$i_{pv} = I_{ph} - I_s \left[e^{\left(\frac{v_{pv} + i_{pv} R_s}{A N V_t} \right)} - 1 \right] - \frac{v_{pv} + i_{pv} R_s}{R_{sh}} \quad (1)$$

where i_{pv} represents the module output current (A), I_{ph} represents the photovoltaic current (A), I_s represents the saturation current of the diode (A), v_{pv} represents the module output voltage (V), V_t represents the thermal voltage (V), A represents the ideality factor, R_s represents the series resistance (Ω), R_{sh} represents the parallel resistance (Ω) [6], and N represents the number of series cells in the module.

V_t can be further demonstrated as;

$$V_t = \frac{NkT}{q_e} \quad (2)$$

where N represents the number of cells in a series string, k represents the Boltzmann constant, T represents the absolute temperature of PV string in Kelvin, and q_e represents the electron charge $(1.602 * 10^{-19} C)$.

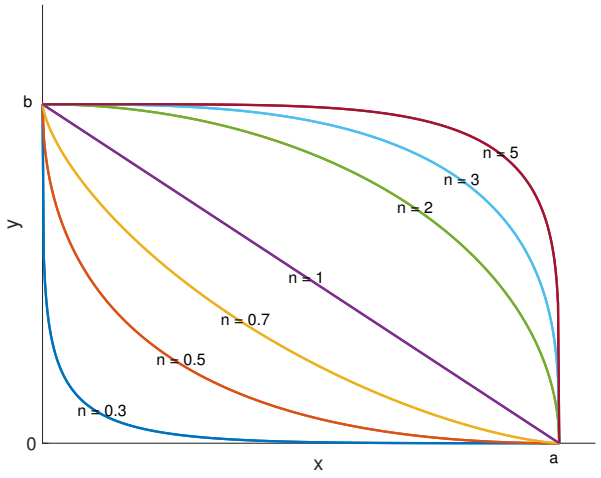


Fig. 4: Typical super-elliptical curves with different n

The photovoltaic current I_{ph} is dependent on both the light intensity and temperature levels of each solar cell. This current can be calculated using

$$I_{ph} = \frac{G}{G_n}\left(I_{scn} + K_I(T - T_n)\right) \tag{3}$$

where I_{scn} represents the short-circuit current at STC(Standard Test Condition: $T_n = 298.15K(25°C)$ in temperature,$G_n = 1000W/m^2$ in insolation condition), T represents the module temperature in Kelvin, G represents the module insolation, and K_I represents the temperature coefficient of I_{sc}.

Another key component of the characteristic equation of the PV panel is the saturation current I_s. I_s can be expressed as;

$$I_s = \frac{I_{scn} + K_I(T - T_n)}{e^{\frac{V_{ocn} + K_V(T - T_n)}{AV_t}} - 1} \tag{4}$$

where V_{ocn} represents the open circuit voltage at STC and K_V represents the temperature coefficient of V_{oc}.

Section I states that the reference signal generated in a SAS depends on the sensed variables., There is a need to find a mathematical equation that approximates the characteristic equation to reduce the cumbersome iterations required due to the implicitness of this signal.

In this regard, the super-elliptical method gives a simple and fast approximation of the I-V characteristic equation. A super-ellipse (or Lamé curve) has a similar curve as an I-V curve. In its first quadrant, both a super-ellipse and an I-V curve have a similar curve, as shown in Fig. 3. As a result, the tangents of this slope at two separate points $(V_{oc}, 0)$ and $(0, I_{sc})$ can then be approximated as zero and an infinite value, respectively.

This basic assumption makes the characteristic equation become a simple mathematical equation. Therefore, applying the Cartesian coordinate system to the curve shown in Fig. 4, the Lamé curve must satisfy the equation:

$$\left|\frac{x}{a}\right|^n + \left|\frac{y}{b}\right|^n = 1. \tag{5}$$

Using (5), an approximated mathematical expression for the PV characteristic equation can then be written as;

$$\left[\frac{v}{V_{oc}}\right]^n + \left[\frac{i}{I_{sc}}\right]^n = 1, (v \geq 0, i \geq 0) \tag{6}$$

In this study, the super-elliptical curve is chosen to go through $(V_{oc}, 0)$,$(0, I_{sc})$, and (V_{mpp}, I_{mpp}). Thus, the value of n can be solved by using the formula

$$\left[\frac{V_{mpp}}{V_{oc}}\right]^n + \left[\frac{I_{mpp}}{I_{sc}}\right]^n = 1 \tag{7}$$

To solve (7), by substituting

$$\left[\frac{V_{mpp}}{V_{oc}}\right] = A, \left[\frac{I_{mpp}}{I_{sc}}\right] = B \tag{8}$$

Hence, the value of n can be obtained by iteration;

$$n_{i+1} = \frac{-B^{n_i}}{\log\left(\frac{A}{B}\right)} \tag{9}$$

where, i represents the iteration index.

Thus, for the super-elliptical curve, the current reference in VS architecture is given as:

$$i_{ref} = I_{sc}\sqrt[n]{1 - (\frac{v}{V_{oc}})^n} \tag{10}$$

where v is the measured output voltage of SAS. Similarly, in the case of CS structure, the voltage reference can be expressed as;

$$v_{ref} = V_{oc}\sqrt[n]{1 - (\frac{i}{I_{sc}})^n} \tag{11}$$

where i_{ref} represents the reference current signal obtained in the VS structure and v_{ref} represents the voltage signal obtained using the CS structure. In addition, i and v are the sensed current and voltage at every instant.

B. Small-signal modeling of a voltage- or current-sensing (VS or CS) reference generator

The reference signal is differentiated with respect to the sensed signal to obtain the small-signal gain of the reference generator. Therefore, the small-signal gain is obtained by differentiating (11) with respect to the sensed current at any given point (V_{op}, I_{op}) in a CS- VRC hardware structure. This small-signal gain is called trans-resistance gain.

$$k_{v_{ref},i} = \frac{\hat{v_{ref}}}{\hat{i}}\Big|_{(V_{op},I_{op})} = -\frac{V_{oc}I_{op}^{(n-1)}}{I_{sc}^n}\left[1 - \left(\frac{I_{op}}{I_{sc}}\right)^n\right]^{(\frac{1}{n}-1)} \tag{12}$$

Similarly, a trans-conductance small-signal gain at point (V_{op}, I_{op}) is obtained by differentiating (10) with respect to the sensed voltage.

$$k_{i_{ref},v} = \frac{\hat{i_{ref}}}{\hat{v}}\Big|_{(V_{op},I_{op})} = -\frac{I_{sc}V_{op}^{(n-1)}}{V_{oc}^n}\left[1 - \left(\frac{V_{op}}{V_{oc}}\right)^n\right]^{(\frac{1}{n}-1)} \tag{13}$$

C. Small-signal modeling of a resistance sensing (RS) reference generator

Two stages are involved when a RS reference generator is involved. Firstly, the instantaneous resistance is obtained by dividing the sensed voltage by the sensed current.

$$r = \frac{v}{i} \tag{14}$$

Secondly, (14) is substituted into (11) and (10), respectively, to obtain the reference signal. Therefore, the reference for RS-VRC and RS-CRC is given, respectively:

$$v_{ref,RS} = \frac{1}{\sqrt[n]{\left(\frac{1}{rI_{sc}}\right)^n + \left(\frac{1}{V_{oc}}\right)^n}}. \tag{15}$$

$$i_{ref,RS} = \frac{1}{\sqrt[n]{\left(\frac{r}{V_{oc}}\right)^n + \left(\frac{1}{I_{sc}}\right)^n}}. \tag{16}$$

The small-signal gain describing the first step of instantaneous resistance (14) can be written as:

$$\hat{r} = k_{rv}\hat{v} + k_{ri}\hat{i} \tag{17}$$

As a result, these two small-signal gains can therefore be represented by differential equations at any operating point;

$$k_{rv} = \frac{\hat{r}}{\hat{v}}\Big|_{(V_{op},I_{op})} = \frac{1}{I_{op}}, k_{ri} = \frac{\hat{r}}{\hat{i}}\Big|_{(V_{op},I_{op})} = -\frac{V_{op}}{I_{op}^2}. \tag{18}$$

Two different cases are to be considered to describe the small-signal model of the actual reference signal. If the reference signal is given as $v_{ref} = f(r)$ as in (15), then the small-signal gain at the operating point (V_{op}, I_{op}) is determined to be;

$$k_{v_{ref},r} = \frac{\hat{v_{ref}}}{\hat{r}}\Big|_{(V_{op},I_{op})} = \frac{1}{r^{1+n}I_{sc}^n\left(\left(\frac{1}{rI_{sc}}\right)^n + \left(\frac{1}{V_{oc}}\right)^n\right)^{\frac{1}{n}+1}} \tag{19}$$

In addition, if the reference signal is of the form $i_{ref} = g(r)$ as represented in (16), then the gain is given to as;

$$k_{i_{ref},r} = \frac{\hat{i_{ref}}}{\hat{r}}\Big|_{(V_{op},I_{op})} = -\frac{r^{n+1}}{V_{oc}^n\left(\left(\frac{r}{V_{oc}}\right)^n + \left(\frac{1}{I_{sc}}\right)^n\right)^{\frac{1}{n}+1}}. \tag{20}$$

From theory, the reference signal in the outer loop must not be faster than the signal generated by the control loop. An intentional time-delay function L(s) is introduced in this model to account for any time-delay effect in the reference signal at any time. In its simplified form, L(s) is given by the first series expansion of the Padé approximation as

$$L(s) = e^{-st_d} \approx \frac{1-\alpha s}{1+\alpha s}; \alpha = t_d/2 \tag{21}$$

where the t_d accounts for such a time delay effect in the reference generation.

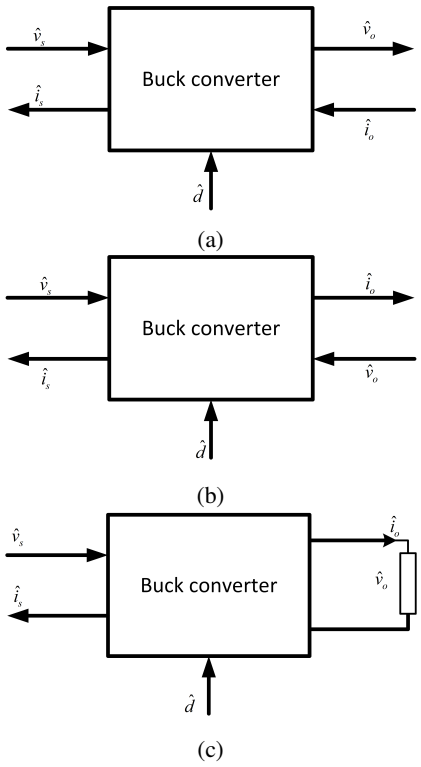


Fig. 5: Block diagrams of converter model (a) Current-terminated model (b) Voltage-terminated model (c) Resistive load-terminated model

III. Modeling and Analysis of SAS systems

To have a clear picture of the dynamics of a SAS, the DC/DC converter model behavior as determined by the connected load, can be represented to be an unterminated converter model having three inputs ($\hat{v_s}, \hat{i_o}$, and $\hat{d}$) and two outputs ($\hat{v_o}, \hat{i_s}$) as shown in Fig. 5. This study assumes a buck converter for the DC/DC power stage; therefore, different small-signal models are obtained under different load configurations.

A. Current-terminated buck converter model

When SAS is connected to the current-sink type of load such as fractional short-circuit current MPPT tracker, the SAS should be modeled as a current-terminated converter.The small-signal model is changed by replacing the load with a current source as shown in Fig. 5a . Hence, the differential output voltage is defined to be

$$\hat{v_o} = dv_o(\hat{v_s}, \hat{i_o}, \hat{d}) \tag{22}$$

Thus,

$$\hat{v_o} \cong \frac{\hat{v_o}}{\hat{v_s}}\Big|_{(\hat{i_o},\hat{d})=0}\hat{v_s} - \frac{\hat{v_o}}{\hat{i_s}}\Big|_{(\hat{v_s},\hat{d})=0}\hat{i_s} + \frac{\hat{v_o}}{\hat{d}}\Big|_{(\hat{i_o},\hat{v_s})=0}\hat{d} \tag{23}$$

If a well-regulated power supply provides an input voltage to the buck converter, $\hat{v_s}$ can be determined to be zero. The

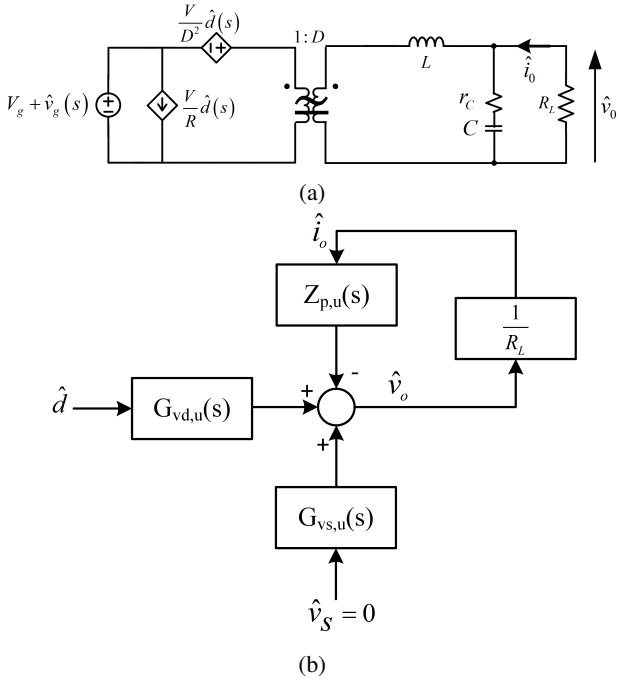


Fig. 6: Resistive load-terminated converter model (a) Equivalent circuit (b) Small-signal model

resulting transfer function for the unterminated voltage source converter is,

$$G_{vd,u}(s) = \frac{\hat{v_o}(s)}{\hat{d}(s)}\Big|_{(\hat{i_o},\hat{d})=0} = V_s \frac{1+sCr_c}{1+sCr_c+s^2LC} \tag{24}$$

$$Z_{p,u}(s) = \frac{\hat{v_o}(s)}{\hat{i_o}(s)}\Big|_{(\hat{i_o},\hat{v_s})=0} = \frac{sL}{1+sCr_c+s^2LC}. \tag{25}$$

B. Voltage-terminated buck converter model

Comparatively, it should be modeled to be a voltage-terminated converter when the SAS is connected to a voltage-sink type load such as the fractional open-circuit voltage MPPT tracker. Applying this same principle to a current source converter shown in Fig. 5b, the resulting unterminated transfer functions are derived as:

$$G_{i_od,u}(s) = \frac{\hat{i_o}(s)}{\hat{d}(s)} = \frac{V_s}{sL} \tag{26}$$

$$Y_{q,u}(s) = \frac{\hat{i_o}(s)}{\hat{v_o}(s)} = -\frac{1+sCr_c+s^2LC}{sL+s^2LCr_c}. \tag{27}$$

C. Resistive load-terminated buck converter model

Similarly, the resistance load-terminated converter model illustrated in Fig. 5c having two transfer functions G_{vd} and G_{i_od}. Fig. 6 shows the canonical equivalent circuit diagram and small- signal models. Note that G_{vd} and G_{i_od} can also be derived using the unterminated model in (24) and (26) [25].

$$G_{vd}(s) = G_{vd,u}(s)\frac{1}{1+\frac{Z_{p,u}(s)}{R_L}} \tag{28}$$

$$G_{i_od}(s) = G_{i_od,u}(s)\frac{1}{1+R_LY_{q,u}(s)} \tag{29}$$

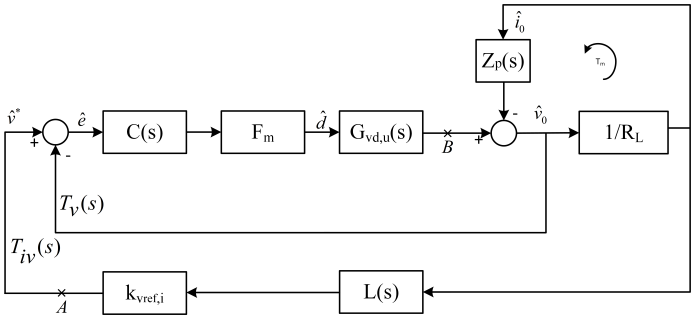


Fig. 7: Small-signal block diagram of the CS-VRC system

The resistance-terminated model equations are derived to be

$$G_{vd}(s) = \frac{\hat{v_o}(s)}{\hat{d}(s)} = V_s \frac{(1+sCr_c)}{1+(Cr_c+\frac{L}{R_L})s+LC(1+\frac{r_c}{R_L})s^2} \tag{30}$$

$$G_{i_od}(s) = \frac{\hat{i_o}(s)}{\hat{d}(s)} = \frac{V_s}{R_L}\frac{(1+sCr_c)}{1+(Cr_c+\frac{L}{R_L})s+LC(1+\frac{r_c}{R_L})s^2} \tag{31}$$

It is known that most MPPT controllers can be considered as constant power load, which shows negative resistance in very low frequency and positive resistance in other frequency regions [26]–[30]. Therefore, this study only considers the positive resistive loads to investigate the dynamic behavior of SAS. However, note that other load conditions can be dealt with similarly.

According to Fig. 1, a controller is also required for the smooth running of a SAS. Therefore, in this study, a type III compensator C(s) is used and expressed in a mathematical form to be:

$$C(s) = \frac{k_u}{s}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{32}$$

where k_u represents the gain, ω_{z1}, ω_{z2} and ω_{p1}, ω_{p2} are real zeros and poles respectively.

D. Small-signal analysis of current-sensing voltage reference Control (CS-VRC)

Hardware structures look like a single-loop system having only a voltage loop in its basic form. However, a closer look into this structure reveals another time-varying loop that is governed by the sensed current, as shown in Fig. 7. This essentially transforms the system into a multi-loop system where the voltage and reference loops form the inner and outer loop of the system, respectively.

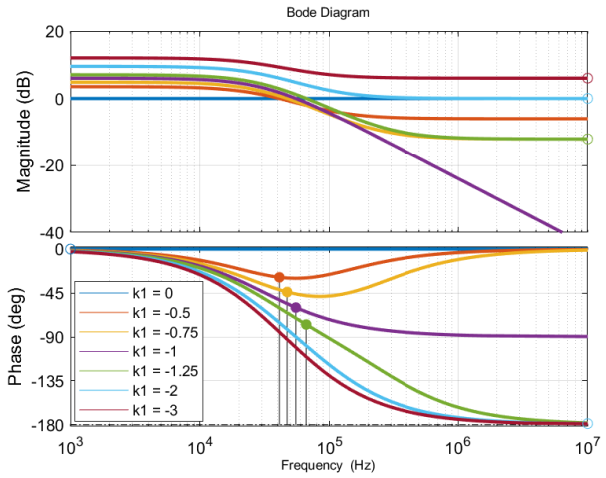
Therefore, the loop gains for each loop can be derived as follows;

$$T_v(s) = F_mC(s)G_{vd}(s) \tag{33}$$

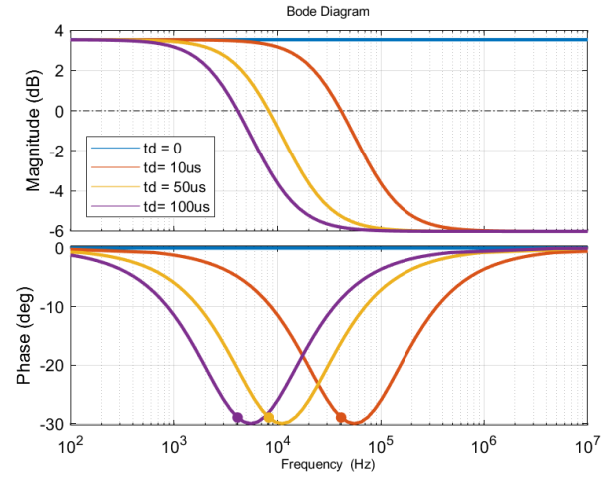
$$T_{iv}(s) \equiv F_mC(s)G_{vd}(s)\frac{k_{v_{ref},i}L(s)}{R_L} \tag{34}$$

where $k_{v_{ref},i}$ represents the gain defined in (12), and L(s) represents the time delay function in (21).

However, the overall loop gain is not uniquely defined in the multi-loop system, but defined by either the signal injection



(a)



(b)

Fig. 8: Loop interaction function $K_1(s)$ (a) according to k_1 when t_d=10μs (b) according to t_d when k=-0.5

point or the breaking point [25], [31]. Therefore, special consideration is needed. If the overall loop is intercepted at a point A as shown in Fig. 7, then the outer loop gain is obtained as;

$$T_A(s) = \frac{T_{iv}(s)}{1 + T_v(s)}. \tag{35}$$

Similarly, if the loop is interrupted at point B, then the overall loop gain is derived to be:

$$T_B(s) = T_v(s) + T_{iv}(s). \tag{36}$$

This study focuses on the overall loop gain $T_B(s)$ to analyze the loop interactions within the multi-loop systems. By substituting (34) and (33) into (36), we obtain;

$$T_B(s) = F_m C(s) G_{vd}(s) K_1(s) \tag{37}$$

where $K_1(s)$ represents the degree of interference from the outer loop and is defined as;

$$K_1(s) = (1 - k_1 L(s)); k_1 = \frac{k_{v_{ref},i}}{R_L} \tag{38}$$

If the value of $K_1(s)$ is unity, then no interactions exist between the inner and outer loops. Hence, this system is seen as a single loop. Practically, the determinant factors for calculating the value of $K_1(s)$ are the resistance ratio k_1 and the time delay function L(s).

k_1 is the ratio of incremental resistance of the PV curve to the load resistance at every instant by definition. This value is always negative and exhibits the following trends:

$$\begin{aligned}(V_{op}, I_{op}) &\rightarrow (V_{OC}, 0) : k_1 \rightarrow 0\,(< 0)\\ (V_{op}, I_{op}) &\rightarrow (V_{mpp}, I_{mpp}) : k_1 \rightarrow -1\\ (V_{op}, I_{op}) &\rightarrow (0, I_{SC}) : k_1 \rightarrow -\infty\end{aligned}$$

From this trend, it can be concluded that the value of k_1 becomes a very small negative value when it operates either near the open circuit condition or in the voltage source segment (VSS). While k_1 becomes a very large number (approaching negative infinity) when either operating under short circuit conditions or in the CSS.

L(s) is the intentional time-delay effect introduced into the reference signal of a SAS as introduced in Section II.C. To effectively examine the effect of the loop interactions, the mathematical expression for K_1 is rearranged using the Padé approximant in (21) as;

$$K_I(s) = (1 - k_1)\frac{1 + \frac{\alpha(1+k_1)s}{(1-k_1)}}{1 + \alpha s}. \tag{39}$$

Figure 8 shows the simulation results describing the effect of varying k_1 and L(s) on the overall loop gain in the frequency domain. First, by taking a constant time-delay $t_d = 10\mu$s and varying the values of k_1, the result of this variation is shown in Fig. 8a. A small loop interaction was observed in the system due to the presence of a left-half plane zero and small phase angle delay when $-1 < k_1 < 0$. As the SAS operates under MPP, this left-half plane zeros diminish when $k = -1$. Nevertheless, the SAS operates in the CSS when $k_1 < -1$, hence a right-half plane zero is observed, resulting in a remarkable phase angle delay in the system. This increased phase delay reduces the overall system stability of the SAS.

Another possibility is to maintain the value of $k_1 = -0.5$ constant while varying t_d shown in Fig. 8b. The overall stability of the SAS deteriorates if an inappropriate time delay is added to the system, even at a fixed operating point.

E. Small-signal analysis of voltage-sensing current reference control (VS-CRC)

In the VS-CRC hardware structure, the main control loop is the current loop since the sensed voltage is used to generate the reference current. The loop gain at breaking point B as shown in Fig. 9 can be expressed as;

$$T_B(s) = T_i(s) + T_{vi}(s) \tag{40}$$

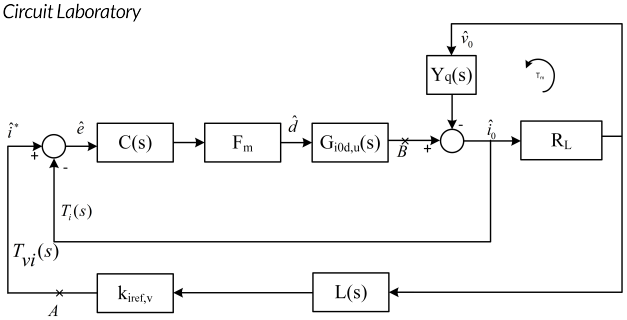


Fig. 9: Small-signal block diagram of the VS-CRC system

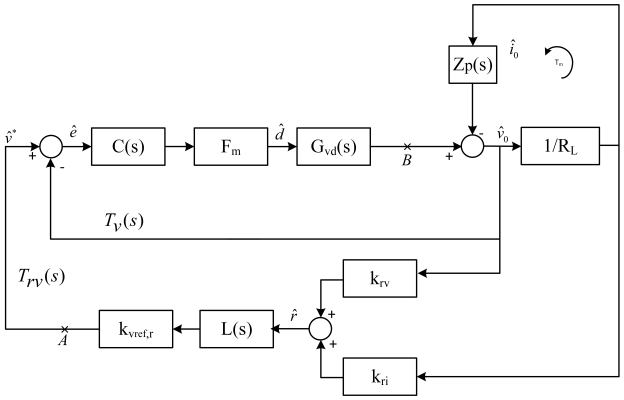


Fig. 10: Small-signal block diagram of the RS-VRC system

where the individual loop gains are derived as:

$$T_i(s) = F_m C(s) G_{iod}(s) \tag{41}$$

$$T_{vi}(s) \equiv F_m C(s) G_{iod}(s) R_L k_{i_{ref},v} L(s) \tag{42}$$

Hence, the small-signal model equation for the overall loop gain is given as;

$$T_B(s) = F_m C(s) G_{iod}(s) K_2(s) \tag{43}$$

where $K_2(s)$ defines the degree of interference between the inner loop and the reference signal.

$$K_2(s) = 1 - k_2 L(s); k_2 = k_{i_{ref},v} R_L \tag{44}$$

Unlike the CS-VRC hardware structure, the resistance ratio (k_2) in (44) is only proportional to the load resistance (R_L) and has the following trends:

$$\begin{aligned}(V_{op}, I_{op}) &\to (V_{OC}, 0) : k_2 \to -\infty \\ (V_{op}, I_{op}) &\to (V_{mpp}, I_{mpp}) : k_2 \to -1 \\ (V_{op}, I_{op}) &\to (0, I_{SC}) : k_2 \to 0\,(< 0)\end{aligned}$$

These operating point characteristics of K_2 are the exact opposite of K_1. Similarly, K_2 can also be approximated by using the Padé approximation as

$$K_2(s) = (1 - k_2)\frac{1 + \frac{\alpha(1+k_2)s}{(1-k_2)}}{1 + \alpha s} \tag{45}$$

As a result, it can be concluded that the VS-CRC system suffers from loop interactions in VSS due to the low phase margin near the open circuit point.

F. Small-signal analysis of resistance-sensing voltage reference control (RS-VRC)

Figure 10 shows the small-signal block diagram for the hardware structure for a RS-VRC, where the current and reference loop gains can be written as;

$$T_v(s) = F_m C(s) G_{vd}(s) \tag{46}$$

$$T_{rv}(s) = -F_m C(s) G_{vd}(s) k_{v_{ref},r} \left(k_{rv} + \frac{k_{ri}}{R_L}\right) L(s) \tag{47}$$

Hence, the overall

$$T_B(s) = F_m C(s) G_{vd}(s) K_3(s) \tag{48}$$

TABLE II: Converter components and Type III controller parameters

Parameter	Value	Unit	Parameter	Value	Unit
V_S	60	V	ω_{z1}	4.4	krad/s
L	210	μH	ω_{z2}	8.8	krad/s
R_l	2	Ω	ω_{p1}	314	krad/s
C	47	μF	ω_{p2}	6.89	Mrad/s
r_c	3.1	$m\Omega$	ω_s	628.3	krad/s
k_u(VRC)	50	rad/s	f_s	100	kHz
k_u(CRC)	550	rad/s			

where

$$K_3(s) = 1 - k_{v_{ref},r}\left(k_{rv} + \frac{k_{ri}}{R_L}\right) L(s) \tag{49}$$

and $k_{v_{ref},r}$ is the small-signal gain in (19) according to the slope of the solar panel curve.

Since the following equality must hold true,

$$k_{rv} + \frac{k_{ri}}{R_L} = \frac{1}{I_{op}} - \frac{V_{op}/I_{op}^2}{V_{op}/I_{op}} = 0, \tag{50}$$

we can get that $K_3(s) \equiv 1$. Resistance-sensing reference generation nullifies the effect of loop interactions within a multi-loop system regardless of variations in either the operating point or time-delay effects in reference signals. This is considered a salient advantage based on the overall system stability.

G. Small-signal analysis of resistance-based current reference control (RS-CRC)

The RS-CRC hardware is dual to the RS-VRC as shown in Fig. 11. The gain of the current and reference loops can therefore be written as

$$T_i(s) = F_m C(s) G_{iod}(s) \tag{51}$$

$$T_{ri}(s) \equiv F_m C(s) G_{iod}(s) L(s) k_{i_{ref},r}\left(k_{ri} + k_{rv} R_L\right) \tag{52}$$

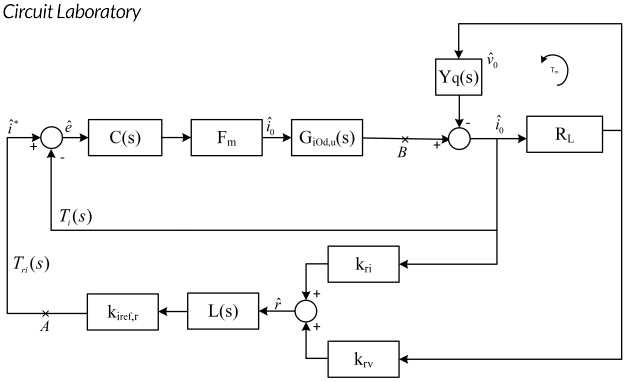


Fig. 11: Small-signal block diagram of the RS-CRC system

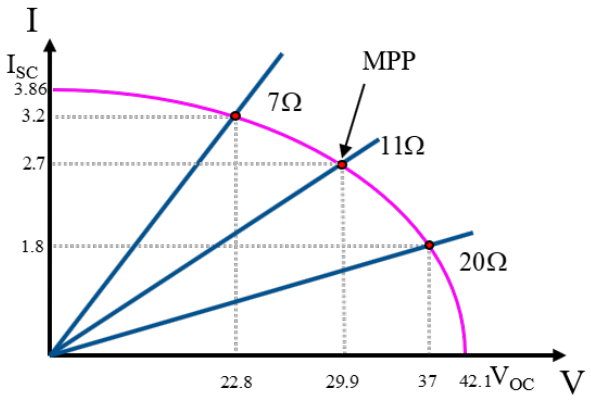


Fig. 12: Operating point and load resistance set-up for verification on the approximate PV curve for MSX120

Consequently, the overall loop gain becomes;

$$T_B(s) = F_m C(s) G_{iod}(s) K_4(s) \tag{53}$$

where

$$K_4(s) = 1 - k_{i_{ref},r}\left(k_{ri} + k_{rv} R_L\right) L(s). \tag{54}$$

Also, the value for $K_4(s)$ becomes unity since

$$k_{ri} + k_{rv} R_L = -V_{op}/I_{op}^2 + \frac{1}{I_{op}} \frac{V_{op}}{I_{op}} = 0. \tag{55}$$

In addition, this result also confirms the ability of the resistance-sensing reference generator to nullify the effect of variations in operating points in a SAS.

IV. Performance Analysis

This Section evaluates the four SAS hardware structures discussed in Section III under varying operating point conditions. In addition, both the frequency and time domain analysis is carried out, thereby justifying the theoretical results observed in the small-signal models.

A. Frequency-domain analysis

Each SAS structure is arranged as shown in Figs. 7, 9, 10 and 11 to evaluate the SAS in the frequency domain. In addition, Tables II and III show the design parameters for the buck converter and PV panel specifications, respectively. The approximate I-V curve using the proposed super-elliptical method in Section II is shown in Fig. 12 indicating both V_{oc} and I_{sc} based on the PV specifications for MSK120.

TABLE III: PV module parameters (MSX120) [32]

Parameter	Value	Unit
P_{Max}	120	W
V_{oc}	42.1	V
I_{sc}	3.87	A
V_{mpp}	33.7	V
I_{mpp}	3.56	A

Three different load resistances, 7Ω, 11Ω, and 20Ω, are chosen to evaluate the stability of the system in the CSS, MPP, and VSS, respectively. Under each condition, the inner loop gains $T_v(s)$, $T_i(s)$ and the overall loop gain $T_B(s)$ are evaluated, and the simulation results are shown in both Fig. 13 and Fig. 14.

In the CS-VRC structure, the operating point shifts towards the CSS with a decrease in the load resistance, resulting in the increase in both the loop gain and gain cross-over frequency. Therefore, a significant loss in the phase margin is observed as shown in Fig. 14a. Comparatively to this, under the RS-VRC hardware structure shown in Fig. 14c, the loop gain change is quite insignificant for the three load resistances.

The loop characteristics of CRC are more load-dependent than VRC based on simulation results in Fig. 14b and 14d. However, RS-CRC is far less sensitive when compared with VS-CRC, thus making the overall loop gain behave in a similar fashion described in Fig. 13b.

B. Time-domain analysis

The time-domain analysis of these SAS configurations is carried out on PSIM by using the average buck converter models shown in Fig. 15. Two load resistances are connected in parallel to give the desired load disturbance to simulate results accurately. Furthermore, the load resistances are adjusted by approximately 40% in both directions at each operating point. The overall step-response waveform is illustrated in Fig. 16.

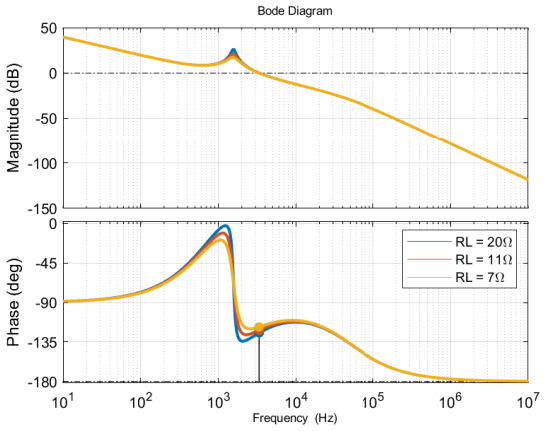
Different load tests are carried out since CRC, and VRC hardware structures become load-dependent at VSS and CSS. The step-down load test is performed in VRC, while the step-up load test is carried out in CRC. The simulated results under step-load changes are shown and marked in Fig. 16. In addition, a summarized result of the dynamic performance of the SAS system under varying operating points is shown in Fig. 17 and Table IV.

According to the small-signal analysis in Section III, the VRC system is expected to have a small phase margin at a low resistive load. In accordance with this prediction, in the CS-VRC system shown in Fig. 16a, as the load decreases from

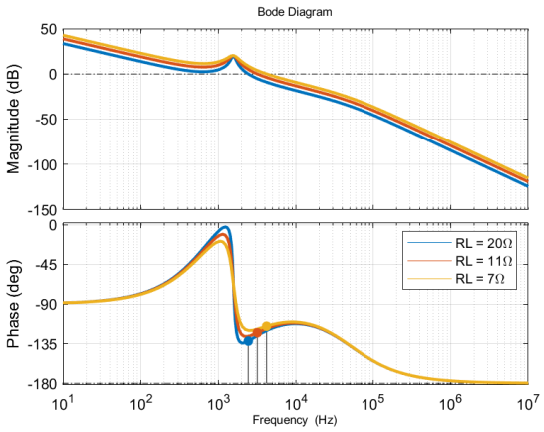
TABLE IV: Simulation results

Operating point	Current segment		MPP		Voltage segment	
System	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)
CSVRC	1.9^*	2.2	1.3^*	0.7	0.2^*	0.4
RSVRC	0^*	0.9	0^*	1.0	0^*	0.4
VSCRC	0.8	0.3	1.5	0.8	10	9.3
RSCRC	0.5	0.3	0.3	0.9	0.8	1.8

$*^*$ = undershoot



(a)



(b)

Fig. 13: Bode diagrams of the inner loop gain (a) $T_v(s)$ in VRC (b) $T_i(s)$ in CRC

20Ω to 7Ω, the settling time is increased from 0.27ms to 2.1ms, and the phase margin is reduced, resulting in an undershoot in the output. The system shows under-damped oscillations in the condition of low resistance since the phase margin is not sufficient.

Whereas, the response of the RS-VRC system illustrated in Fig. 16c shows that regardless of different operating points, the settling time changes only slightly from 0.3ms to 0.9ms without severe oscillations. This tendency matches well with the expected results indicating the operating point insensitivity of the RS-VRC configuration mentioned in Section III.D.

Similarly, VS-CRC and RS-CRC systems are compared to demonstrate theoretical predictions established in the small-signal modeling. In this case, the load resistance is tested in ascending order from 7Ω to 20Ω, considering a more stable operation in VSS. In addition, Fig. 16b and 16d show that the output response is the same under the VRC hardware structure. According to the duality between RS-CRC and VS-CRC configurations, the system stability deteriorates at high load resistance, and RS-CRC is less sensitive to changes in the operating point than VS-CRC.

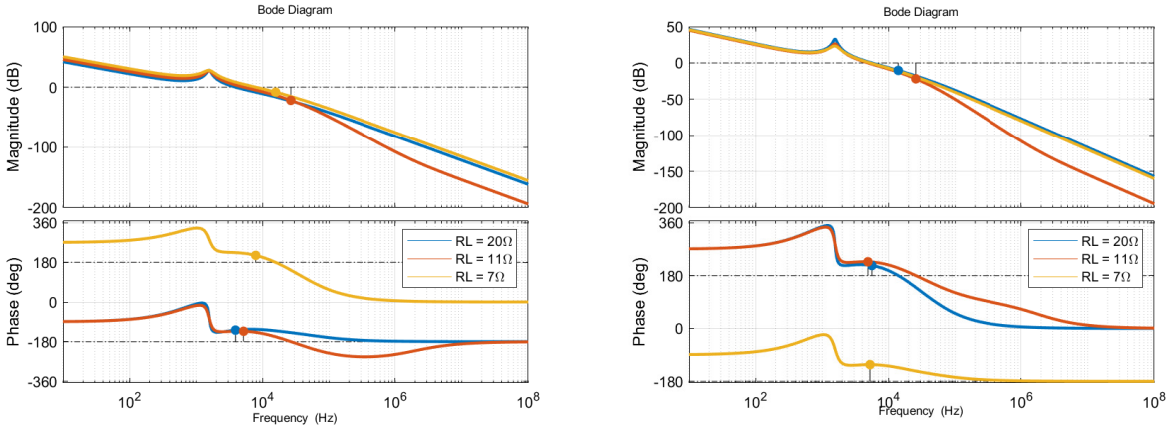
Despite RS-CRC showing similar trends to RS-VRC, its dynamic response is relatively sensitive to the operating point variations because the power stage transfer function has load-dependent dc-gain characteristics. Therefore, RS-VRC appears to be the best configuration in terms of load-independent dynamic characteristics. This confirms the validity of the comparison based on the small-signal analysis presented in this study.

V. Experimental Verification

Figure 18 shows the setup for the hardware verification of the SAS control structures. The SAS is made up of a buck converter incorporated with a TMS320F28379D DSP controller. Variable load resistances are also connected in parallel with the SAS system for step load change to verify the same scenarios. Figs. 19 to 22 and Table V show the experimental results obtained.

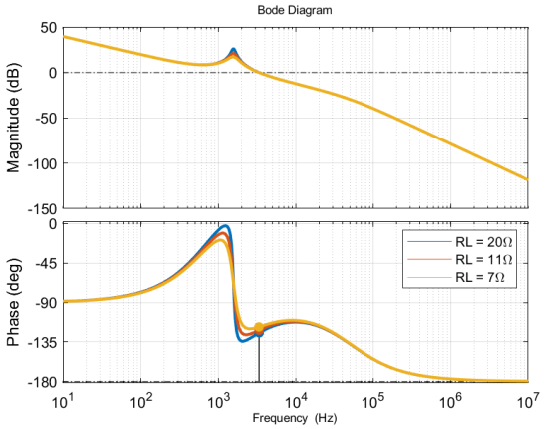
The settling time in the CS-VRC hardware structure fluctuates as the undershoot becomes more prominent due to small load resistance. This underdamped oscillation becomes very pronounced for the 7Ω as shown in Fig. 19. In addition, the RS-VRC hardware system has a minimal undershoot with an almost constant settling time, as shown in Fig. 20. Thus proving that CSS is the worst-case scenario for a CS-VRC, while the stability of CS-VRC structures is load-dependent, the RS-VRC shows an almost constant dynamic response under varying load conditions.

Furthermore, the CRC hardware structures shown in Figs. 21 and 22 also show similar behavior as discussed in Section

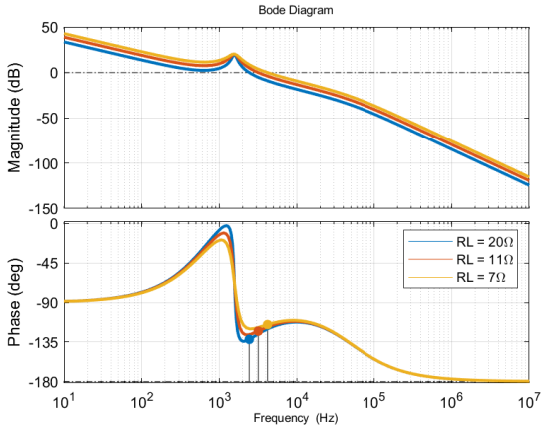


(a)

(b)



(c)



(d)

Fig. 14: Bode diagrams of the overall loop gain $T_B(s)$ (a) CS-VRC (b) VS-CRC (c) RS-VRC (d) RS-CRC

TABLE V: Hardware results

Operating point	Current segment		MPP		Voltage segment	
System	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)
CSVRC	1.5*	oscillatory	1*	1.3	1.0*	0.8
RSVRC	0*	0.8	0.5*	0.9	0.5*	0.8
VSCRC	0.5	0.4	1.5	1.6	2.5	1.6
RSCRC	0.5	0.4	0.5	1.0	1.0	1.1

$*^*$ = undershoot

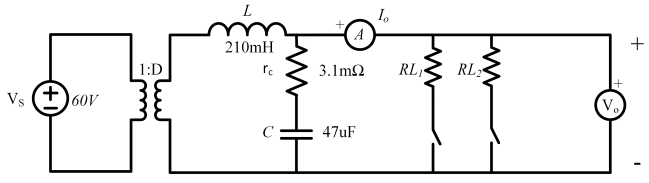


Fig. 15: Average buck converter model

IV.B. The experiment starts from a low resistance load (7Ω) to a very high resistance load (20Ω). Low overshoot and settling time were observed at low resistance, while very high overshoot and settling time was observed at high resistance.

Therefore, this confirms that RS-CRC structures can suppress the effect of performance degradation caused by a change in operating point. However, RS-CRC is slightly sensitive to operating point change when compared with RS-VRC hardware structures. Hence, both the simulation and experimental

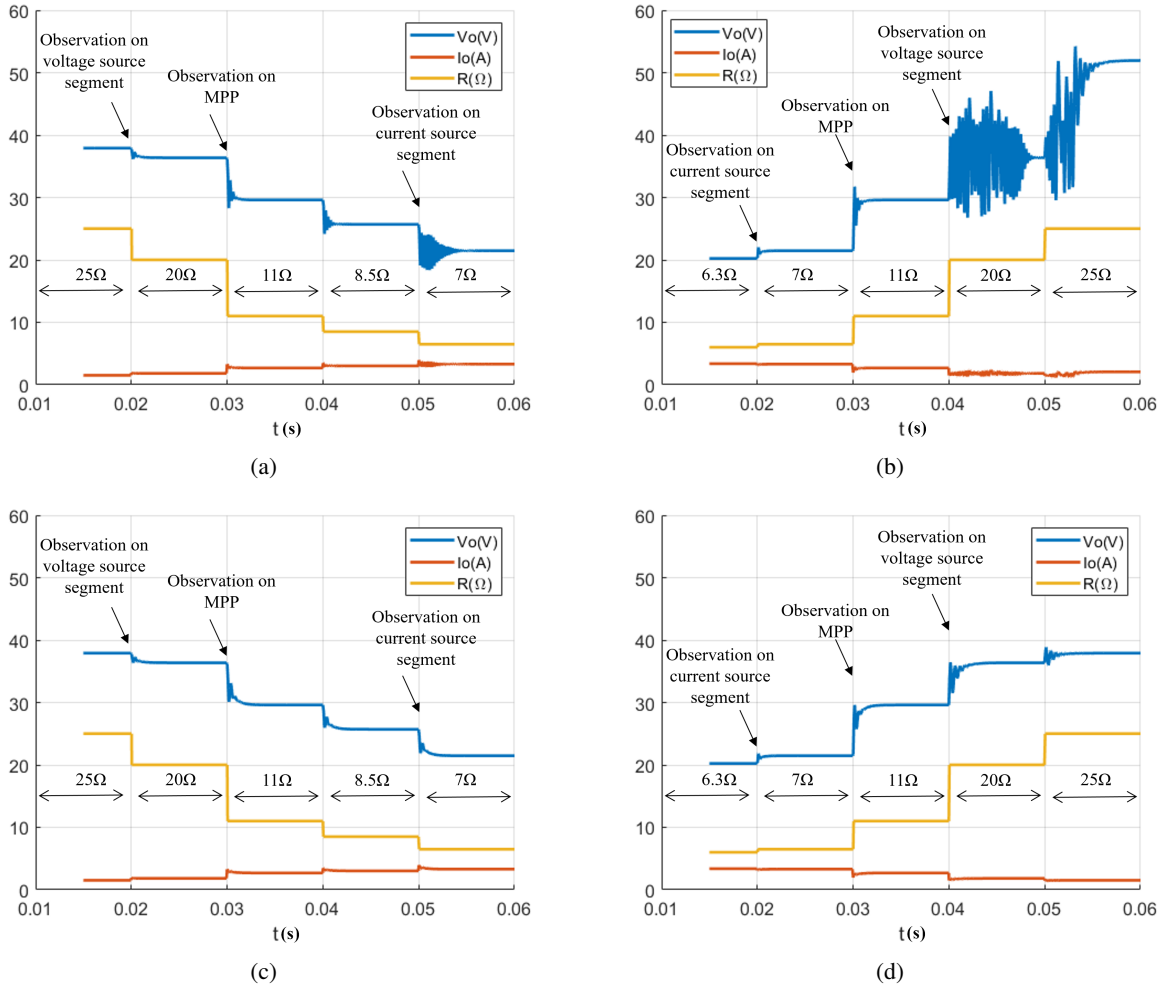


Fig. 16: Step load response for the different configurations used (a) CS-VRC (b) VS-CRC (c) RS-VRC (d) RS-CRC

verification confirm the small-signal analysis results.

Figure 23 shows the output impedance characteristics of the SAS measured by the network analyzer (Ridley Engineering, AP300). It is observed that the phase of the output impedance is not always within +/- 90 degrees, which is different from a real PV generator always exhibiting passive behavior [33]. However, every impedance shows a purely resistive in its low-frequency region like a real PV generator, which indicates that with an appropriate input filter design with damping, system interconnection issue can be avoided considering minor loop gain analysis suggested by [34]. It should be noted that the system interaction issue is yet to be discussed in this paper and thus will be our future work.

VI. Conclusion

In this study, the small-signal modeling and stability analysis of SAS was examined using the multi-loop analysis technique. The super-elliptical method was proposed as a fast and straightforward method for approximating the I-V curve to simplify the I-V characteristic equation. It was also shown that SAS is a multi-loop system consisting of an inner control loop and reference generator loop and the overall loop gain is heavily dependent on the operating point due to the interactions between these two loops. For a use case of the approximate analysis, four SAS hardware structures are examined and compared to investigate the effect of the operating point variation on the dynamic performance, which shows the RS-VRC hardware structure more robust and insensitive to load fluctuations. In conclusion, the proposed approach is expected to be very helpful in improving the control and performance of SAS systems.

Acknowledgment

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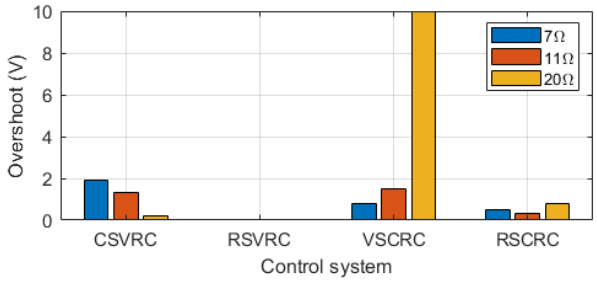
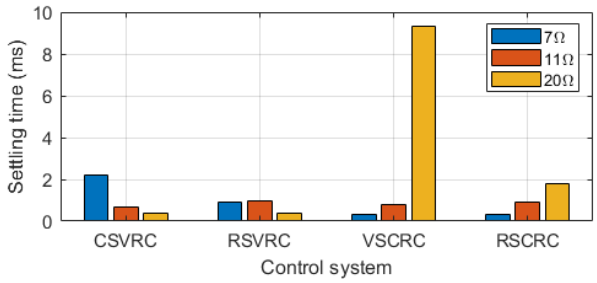
Appendix A
Accuracy of super-elliptical approximation for PV curve

Fig. 24 illustrates the I-V and P-V curves to validate the feasibility of the super-elliptical model. The results confirm that super-elliptical approximation is almost as accurate as of the single diode model.



(a)



(b)

Fig. 17: Simulation results (a) Overshoot (b) Settling time

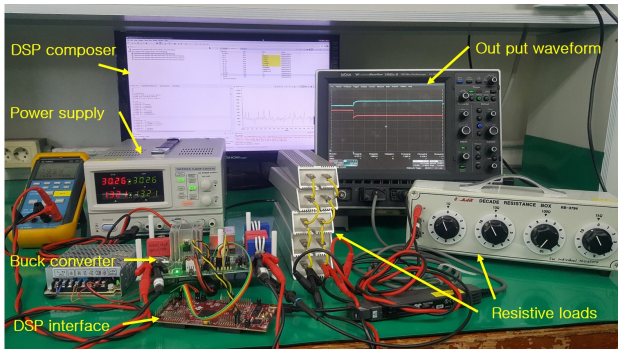


Fig. 18: Hardware setup of SAS

To prove the PV model accuracy quantitatively, Table VI summarizes the accuracy of two different PV models for four commercial PV panels, compared with datasheet values in terms of PV curve parameters. Even though the super-elliptical model has a slightly higher error of 4%, than the diode model, it is quite acceptable for the analysis of SAS.

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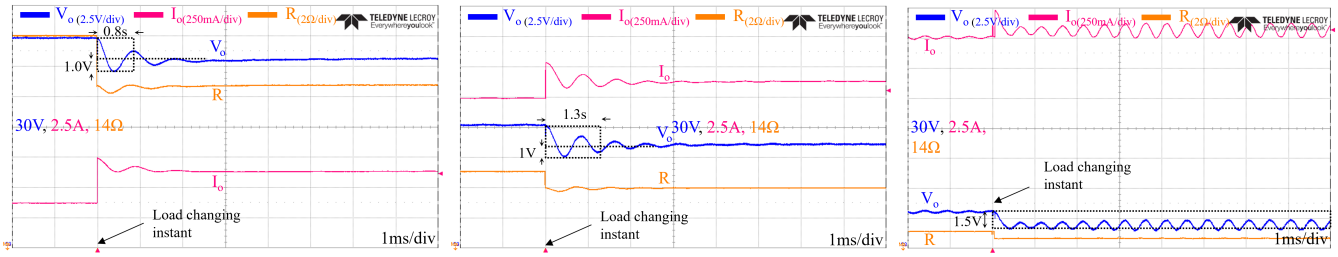
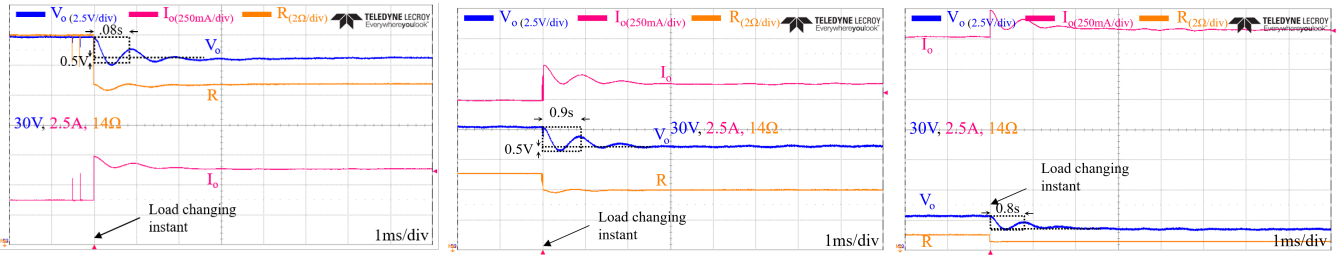


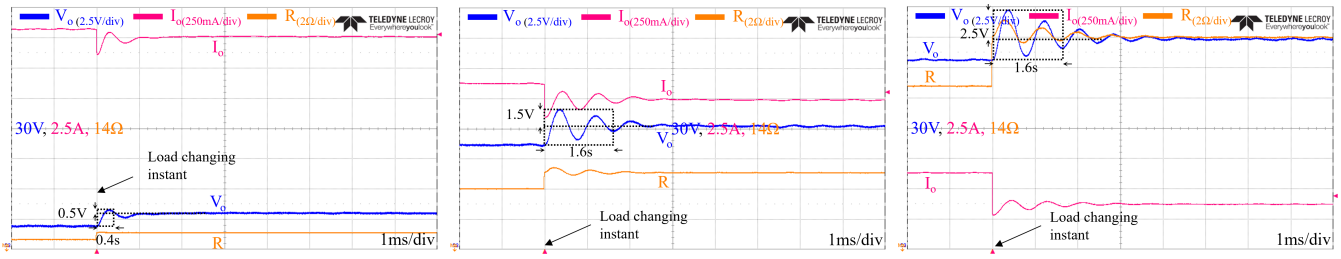
(a) $20\Omega \rightarrow 15\Omega$ (b) $11\Omega \rightarrow 10\Omega$ (c) $7\Omega \rightarrow 6.3\Omega$

Fig. 19: Step response of the CS-VRC hardware prototype



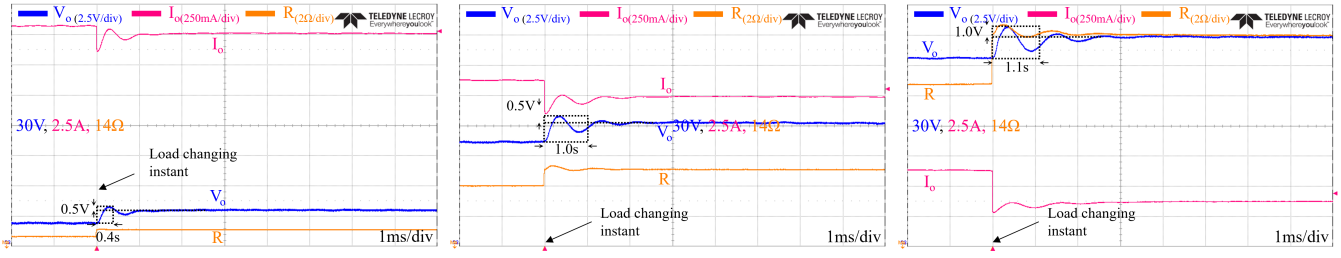
(a) $20\Omega \rightarrow 15\Omega$ (b) $11\Omega \rightarrow 10\Omega$ (c) $7\Omega \rightarrow 6.3\Omega$

Fig. 20: Step response of the RS-VRC hardware prototype



(a) $6.3\Omega \rightarrow 7\Omega$ (b) $10\Omega \rightarrow 11\Omega$ (c) $15\Omega \rightarrow 20\Omega$

Fig. 21: Step response of the VS-CRC hardware prototype



(a) $6.3\Omega \rightarrow 7\Omega$ (b) $10\Omega \rightarrow 11\Omega$ (c) $15\Omega \rightarrow 20\Omega$

Fig. 22: Step response of the RS-CRC hardware prototype

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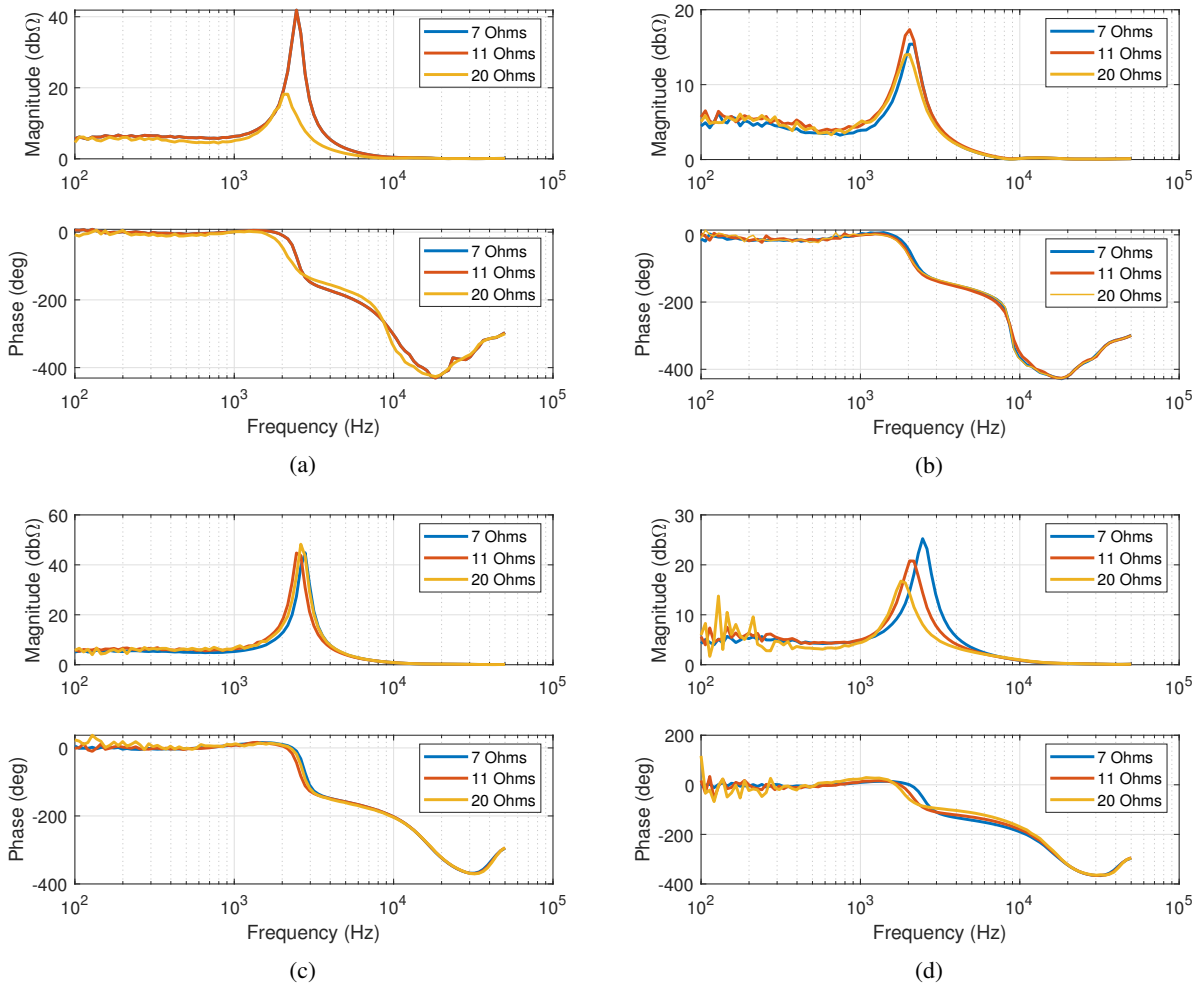

Fig. 23: Measured output impedance of the hardware prototypes (a) CS-VRC (b) VS-CRC (c) RS-VRC (d) RS-CRC

TABLE VI: Comparison of model accuracy

PV module	PV model	P_{mpp} (W)	Error %	I_{mpp} (A)	Error %	V_{mpp} (V)	Error %
	Datasheet	120		3.56		33.7	
	Single diode model	121.45	1.21	3.45	3.19	35.2	-4.26
MSX 120	Super elliptical model (n= 4.9)	122.78	2.32	3.35	6.27	36.6	-7.92
	Datasheet	65		3.75		17.4	
	Single diode model	65.95	1.46	3.6	4.17	18.3	-4.92
KC 65GT	Super elliptical model (n= 5.6)	67.6	4	3.52	6.53	19.2	-9.37
	Datasheet	200		7.61		26.3	
	Single diode model	203	1.5	7.33	3.82	27.7	-5.05
KC 200GT	Super elliptical model (n= 5.1)	205.81	2.90	7.15	6.43	28.8	-8.68
	Datasheet	160		4.58		35	
	Single diode model	162.01	1.26	4.43	3.39	36.6	-4.37
SQ 160-PC	Super elliptical model (n= 5.4)	164.89	3.06	4.31	6.26	38.3	-8.62

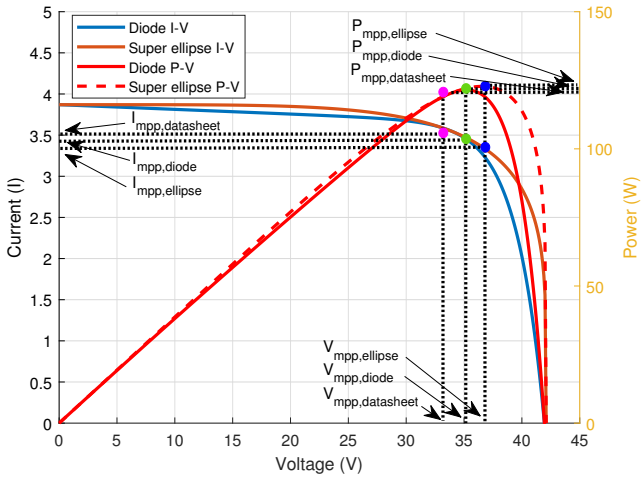

Fig. 24: PV characteristic curves under different PV models

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